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A Pulse-Width Control Loop for Power Electronics Applications

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Abstract

More and more systems use double-sampling or double data rate techniques to ensure electronic products to have high performance and low power dissipation simultaneously. In these systems, a symmetrical clock signal with 50% duty cycle is very important. However, the process, voltage, and temperature variations may change the duty cycle of the used clock. In order to suppress the variations effects, a pulse-width control loop is generally required for these applications. Therefore, in this paper we propose a new control loop which can operate well up to several hundred MHz based on 0.18um CMOS process. Due to the voltage limited charge pump, the lock-time is greatly reduced as compared to other existing prior art circuits. Besides, the acceptable duty range of the input signal varies from 20% to 80%. The validity of the proposed circuit has been verified by test chip results. Therefore, the presented pulse-width control loop can be used for power drives and power electronics applications.

Keywords: Pulse-width; duty cycle; charge pump; lock time; power electronics

1. Introduction

To make electronic products have high performance and low power dissipation simultaneously, more and more systems attend to double-sampling or double data rate techniques. In these systems, a clock signal with 50% duty cycle is required. However, the process, voltage, and temperature（PVT）variations may change the duty cycle of the clock signal. In order to deal with the effects of PVT problems, several pulse-width control loops (PWCL) have been presented [1]-[6].

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For general IC design, a system clock is often needed. However, the duty cycle of the clock signal may be changed through a tapered buffer. Thus, a PWCL circuit is used to fix the duty cycle of the used clock signal. Therefore, the function of PWCL circuits is to stabilize the clock signal and provide a 50% duty cycle output signal at the same time.

2. Existing PWCL circuits

The conventional PWCL [1] is shown in Fig. 1. The conventional PWCL uses a pseudo NMOS inverter to both change and control the duty of the input signal CKin. A ring oscillator and a charge pump circuit CP2 produce a reference voltage Vref. When the duty cycle of CKout is less than 50%, the charge pump CP1 will make the Vc voltage higher than the reference voltage Vref. The output of the operational amplifier（Vctrl）will rise to a higher voltage, so that the PMOS current of the pseudo inverter decreases. Thus the charging time of the pseudo NMOS inverter would become longer. After the driving of the odd inverter chain the duty cycle of CKout will increase. The circuit operations are similar when the duty cycle of CKout is more than 50%. The major difference is that the voltage of Vctrl will decrease and the duty cycle of CKout will also have a tendency to decrease. Finally, Vc equals Vref when the loop is convergent and the signal CKout acquires a 50% duty cycle.

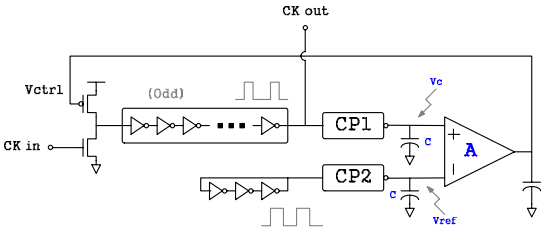

Fig. 1. Conventional PWCL

Another prior art [6] shows a method to design the PWCL circuit, as shown in Fig. 2. The circuit uses a rising edge detector to preset the input clock and make it like a pulse signal. Thus in the same frequency, no mater what the duty cycle of the input, the design condition is always the same. Therefore, the circuit stability will become more reliable.

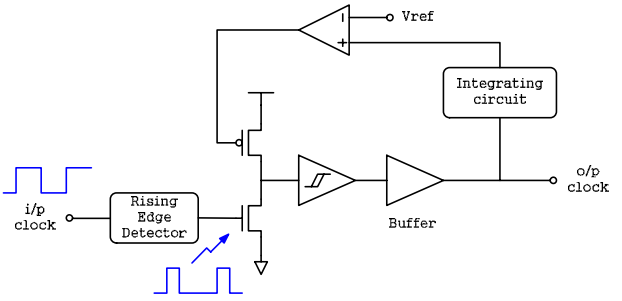

Fig. 2. PWCL of prior art [6]

3. Proposed PWCL

According to the existing PWCL circuits, we take the merits of the prior art circuits and add a voltage limited charge pump to enable the circuit to have faster convergence. Fig. 3 shows the proposed circuit.

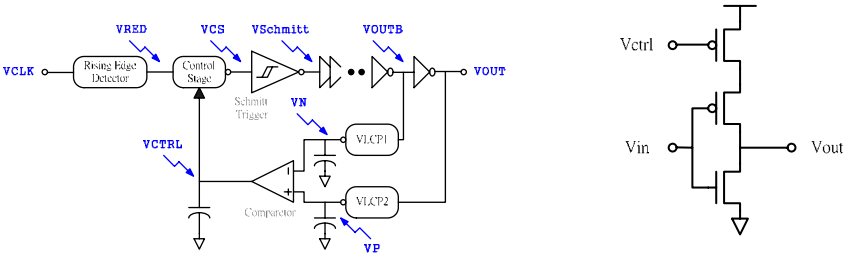

Fig. 3. （a）Proposed circuit （b）Control stage

In Fig. 3(a), the rising edge detector is composed of some inverters and a nand gate. Its frequency is the same as that of the input signal, but its width of the pulse is determined by the delay time. Thus, the output of the rising edge detector VRED, would become a glitch signal whose duty cycle is far less than 50% and the frequency is as large as that of the input clock VCLK. Because of the differential input structure of the comparator, the proposed PWCL has two paths of negative feedback.

The control stage of Fig. 3(b) uses a PMOS switch to isolate the pre-charge current and the discharge current, as shown in Fig. 4. In this design we don't have to worry about the trade-off between the pre-charge and discharge currents. Thus the circuit will be easier to design, but this circuit is not suitable for the condition of duty cycle larger than 50%. Therefore, a rising edge detector is used to both preset the duty cycle and ensure it far less than 50%.

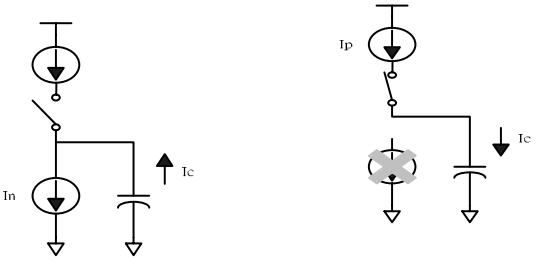

Fig. 4.（a）Discharge of control stage（b）Pre-charge of control stage

In order to decrease the effect of the substrate noise and lower the circuit's mismatch of the comparator, we choose the PMOS differential input pair and use the mirror technique to make the resistance of the input pair to have good matching.

Because of the complementary inputs of the comparator, the offset voltage can be expected to decrease 50%. A traditional PWCL needs a reference voltage signal whose duty cycle equal to 50%. If the comparator has an offset voltage Vos between Vp and Vn, then the offset voltage will totally affect the output duty cycle of the PWCL, but the mutual-correlated structure will share the offset voltage to two input nodes. So the offset can in effect decrease 50% as shown in Fig. 5.

The proposed voltage limited charge pump (VLCP) is shown in Fig. 6. It uses the bounding voltage to replace the initial voltage of the charge pump, so that the convergent time will be decreased because the bounding voltage is closer to the stable voltage than the initial one. To achieve the bounding voltage, we

use an NMOS to pass the logic “high” and a PMOS to pass the logic “low”. Thus when to transmit a “high” signal, the output of VLCP will drop a voltage Vtn and when to transmit a “low” signal, the output of VLCP will rise a voltage |Vtp|. Because of the body effect both Vtn and |Vtp| are larger than their normal values. Therefore, the bounding voltage would be more close to the final stable voltage and therefore decreases the locking time.

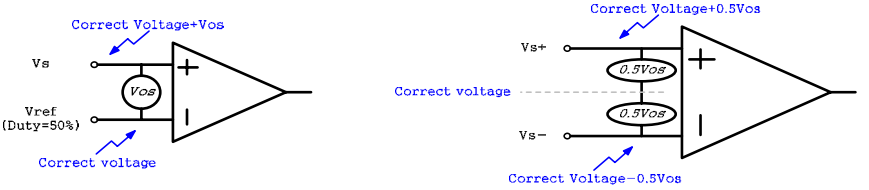

Fig. 5. Effect of the offset voltage for (a) traditional PWCL (b) mutual-correlated PWCL [4]

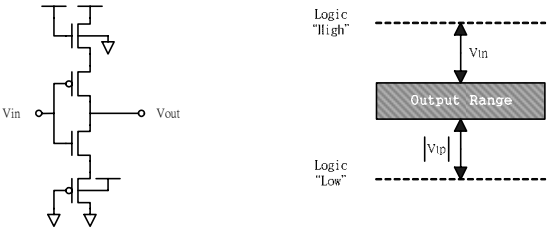

Fig. 6. (a) Proposed voltage limited charge pump（VLCP）(b) Output range of VLCP

4. Simulation results

A 0.18um CMOS process model is used for SPICE simulations. Fig. 7 plots the waveforms at a frequency of 100MHz with 20% duty cycle input. To compare the lock time, we prepare a low-pass filter and a current mode charge pump to replace the proposed VLCP, then compare the convergence time (on the node VCTRL). The simulation results are presented in Fig. 8. It is noted that the proposed circuit has a faster locking operation. A test chip was implemented, as shown in Fig. 9. The verified test results are shown in Fig. 10 and satisfactory good agreement is obtained to confirm the circuit validity.

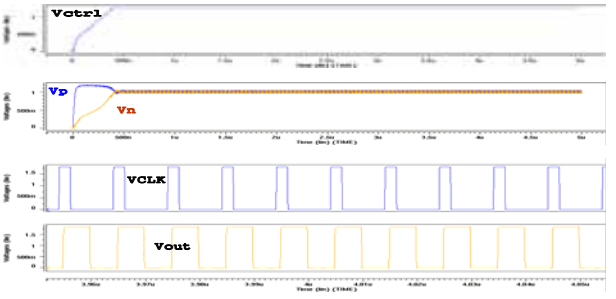

Fig. 7. Simulated circuit operations (VCLK=100MHz with duty cycle=20%)

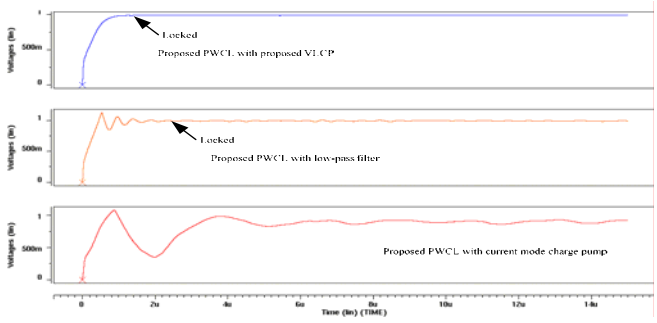

Fig. 8. Simulation results for the lock time performance

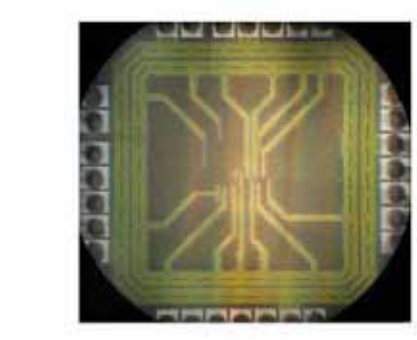

Fig. 9. Die microphotograph of the proposed PWCL

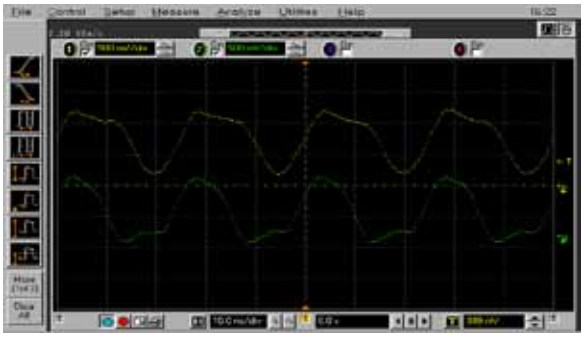

Fig. 10. Measurement results (upper line: 40 MHz input with 60% duty; lower line: output with 50% duty)

5. Conclusion

In this paper, a PWCL with a voltage limited charge pump has been proposed. The proposed voltage limited charge pump is established from the bounding voltage to improve the whole loop convergent

characteristics. Based on simulation results, this design can save the lock time about 0.5us. As the mutual correlated structure used in the proposed PWCL will share the offset voltage between two input nodes of the operational amplifier, we can expect that the proposed PWCL would have the potential capability of reducing the offset voltage. Moreover, using a rising edge detector to preset the duty cycle of the input clock signal ensures the same operating condition for the PWCL insensitive to process variations, so the circuit stability is greatly improved. Furthermore, the validity of the proposed circuit has been verified by test chip results. Therefore, the presented pulse-width control loop can be used for power drives and power electronics applications.

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